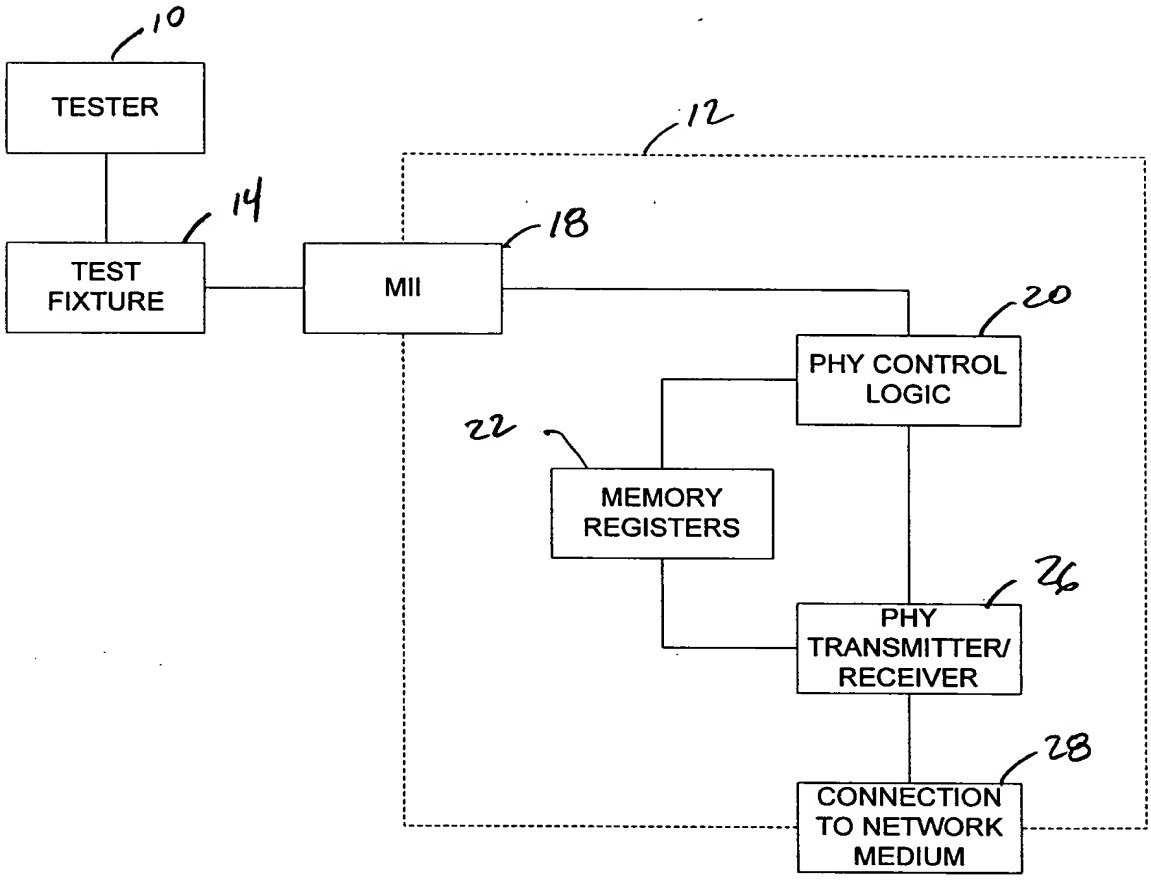
10
TESTER
12
14
TEST FIXTURE
18
MII
20
PHY CONTROL LOGIC
22
MEMORY REGISTERS
26
PHY TRANSMITTER/ RECEIVER
28
CONNECTION TO NETWORK MEDIUM

Fig. 1

18

Pin	Input/Output
TXD0	I
TXD1	I
TXD2	I
TXD3	I
TX_EN	I
TX_ER	I
TX_CLK	O
MDIO	I/O
MDC	I

Pin	Input/Output
RXD0	O
RXD1	O
RXD2	O
RXD3	O
RX_DV	O
RX_ER	O
RX_CLK	O
COL	O
CRS	O

Fig. 2

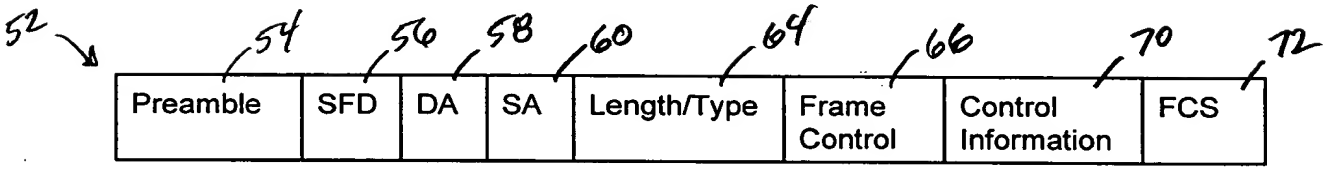

Fig. 3

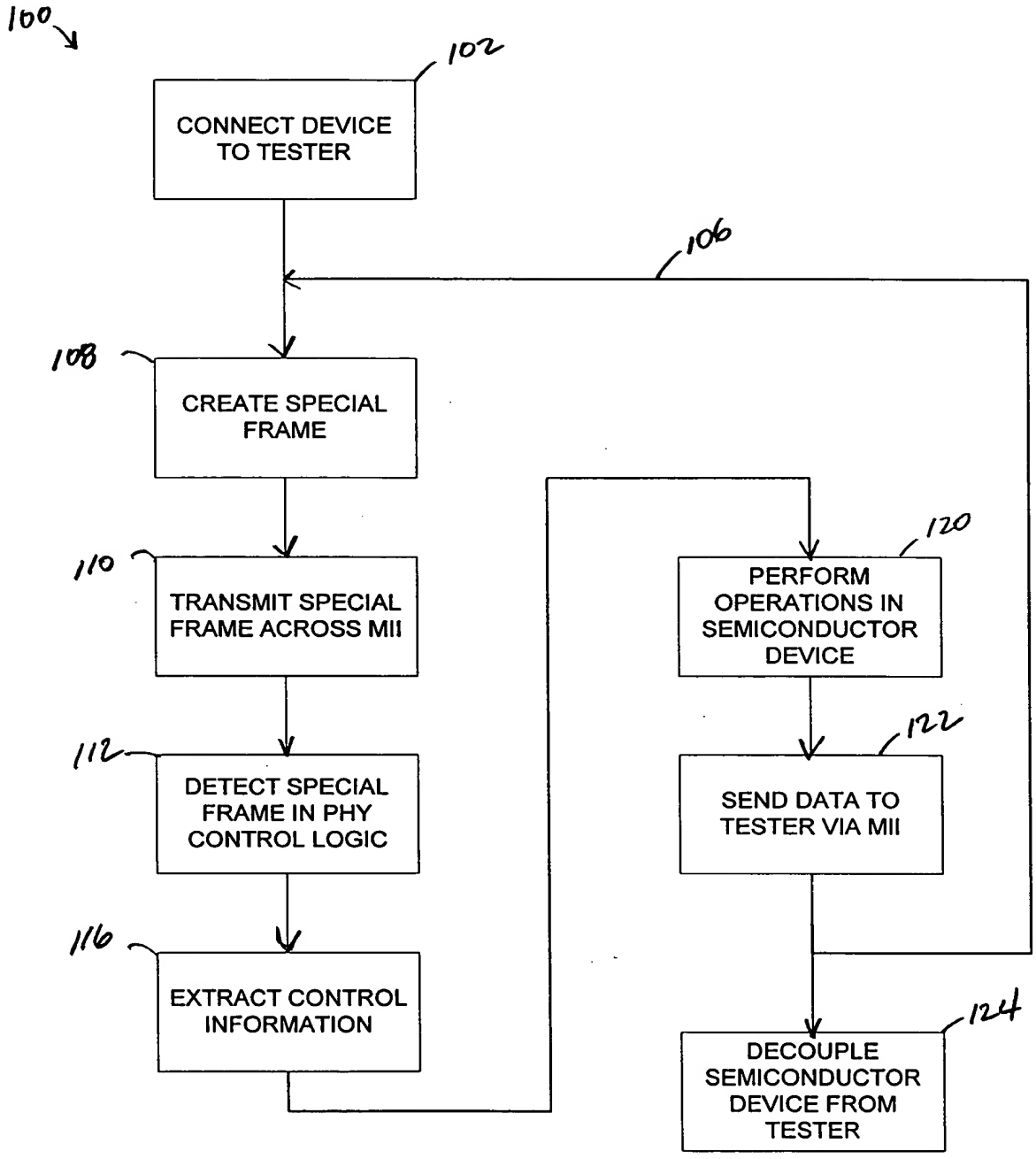
100
102
CONNECT DEVICE TO TESTER
106
108
CREATE SPECIAL FRAME
110
TRANSMIT SPECIAL FRAME ACROSS MII
112
DETECT SPECIAL FRAME IN PHY CONTROL LOGIC
116
EXTRACT CONTROL INFORMATION
120
PERFORM OPERATIONS IN SEMICONDUCTOR DEVICE
122
SEND DATA TO TESTER VIA MII
124
DECOUPLE SEMICONDUCTOR DEVICE FROM TESTER

Fig. 4